Superconducting computing

a beyond-CMOS solution on the way towards quantum computation

Pascal FEBVRE

IMEP-LAHC - CNRS UMR 5130
Université Savoie Mont Blanc
France

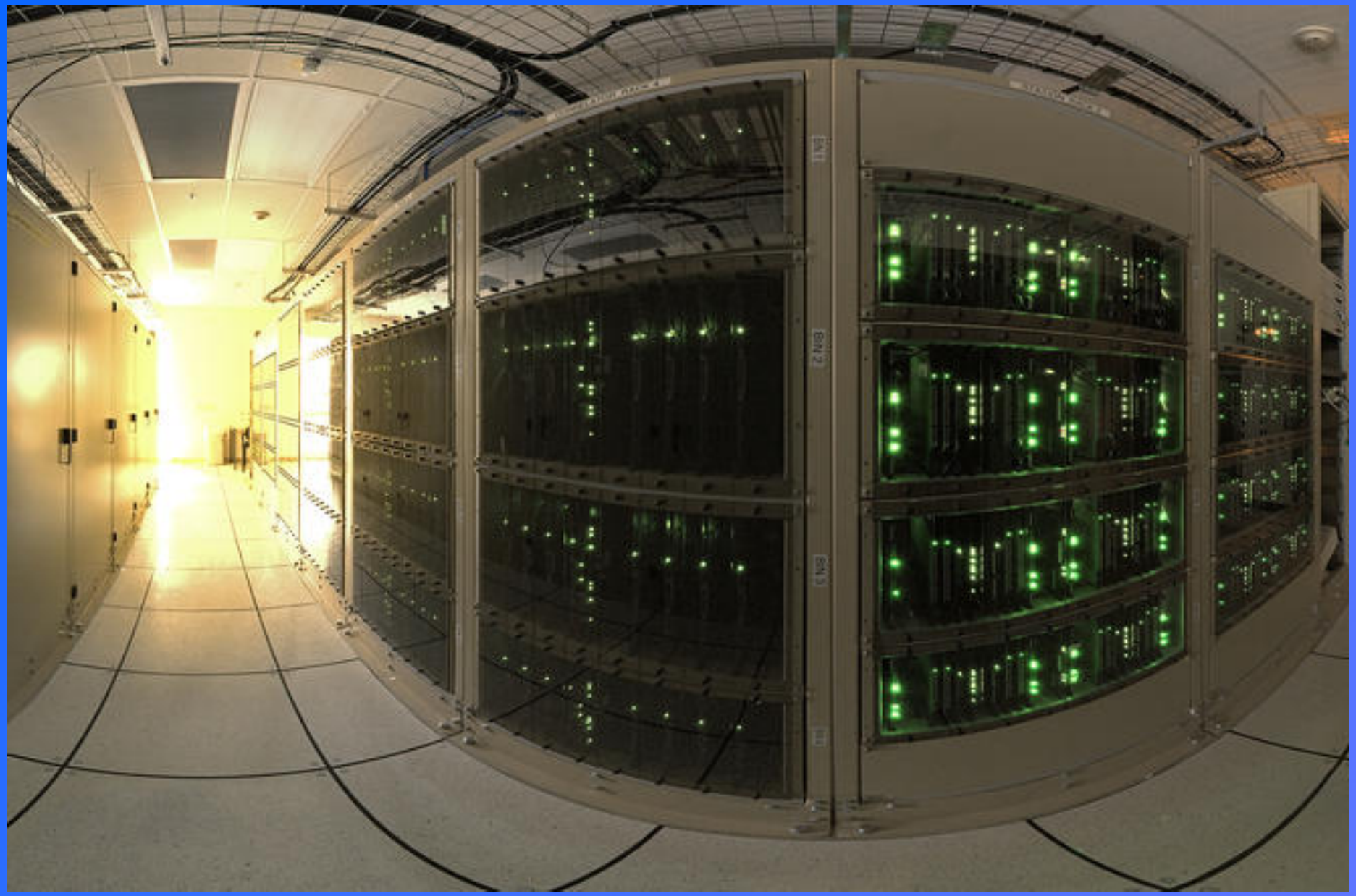
Pascal.Febvre@univ-smb.fr

European FLUXONICS Society

Radioastronomy receivers

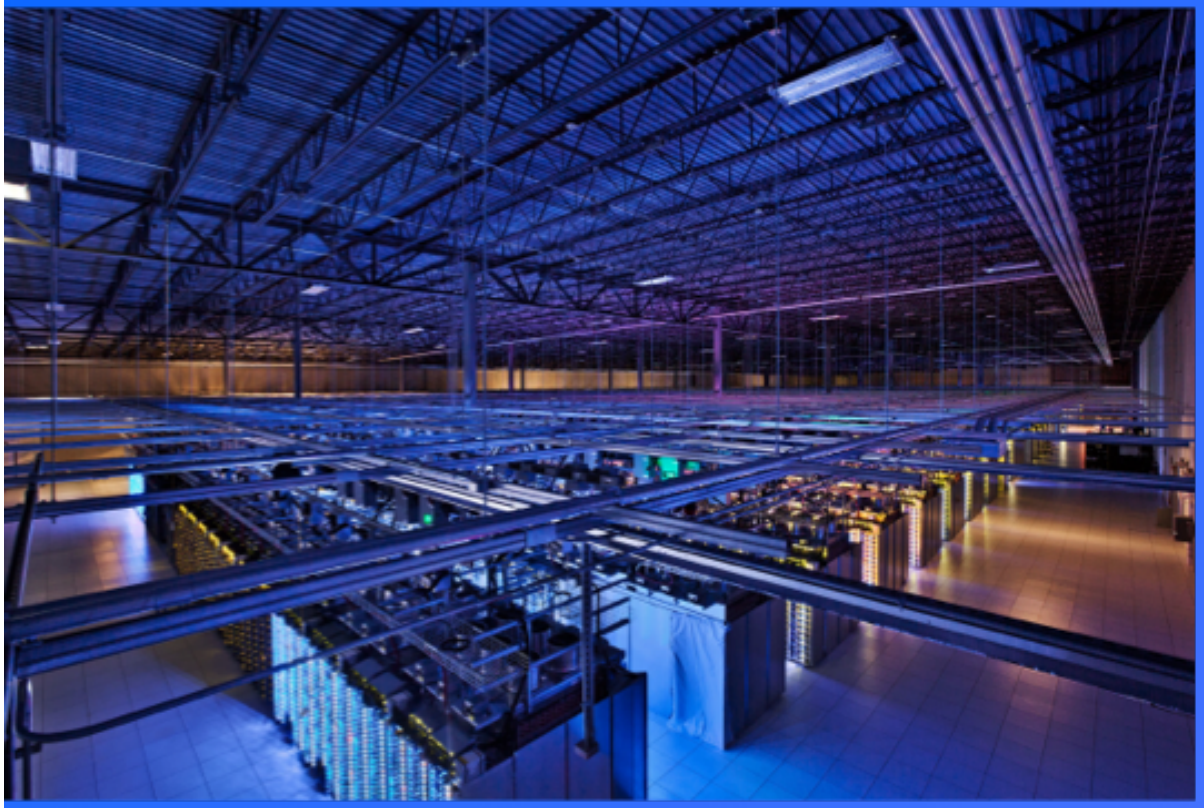
Expérience PIROG8 - récepteur à 424/440 GHz - Observatoire de Paris - Observatoire de Stockholm - CNES - ESA - 1997

ALMA correlator



One of the four quadrants making up the ALMA correlator - Copyright : ESO

Google servers - The Dalles - Oregon



Energy consumption

In 2010, routers and servers consumed :

- between 1.1 % and 1.5 % of the total energy production worldwide
- between 1.7 % and 2.2 % in the United States of America

Copyright Google

Need of computers with higher performance

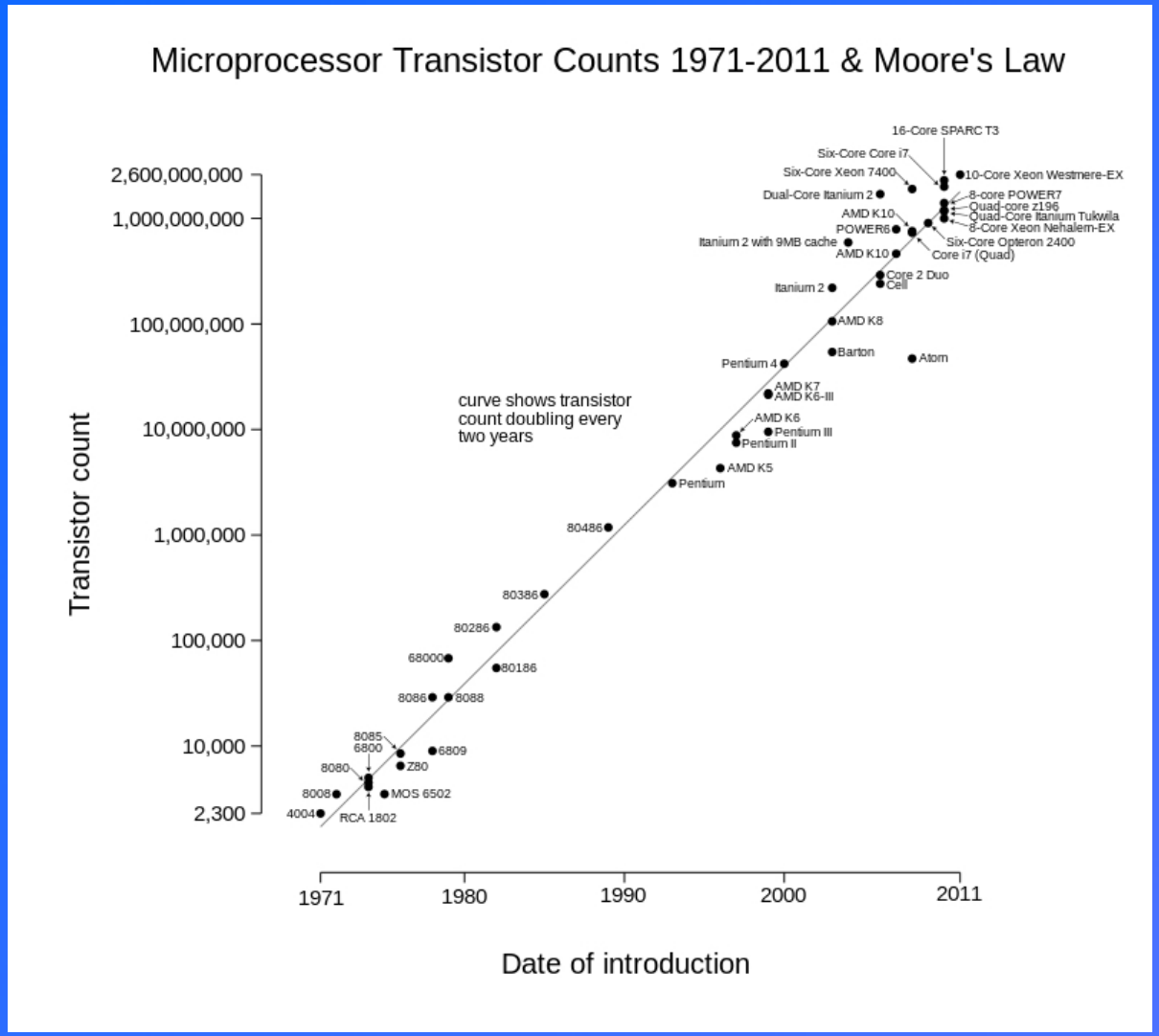
The demand of high performance computers and servers will continue to grow. We need :

- better predictive models for climate change and weather forecast ;
- to better understand the formation of the early Universe ;
- to understand subatomic physics ;
- to model cells, for genetics, biotechnologies ;
- to simulate brain functions, …

But the required power cannot follow the same pace

Pushing current technologies to the limits

Moore's law : the density of transistors per unit area of electronics chips doubles roughly every two years

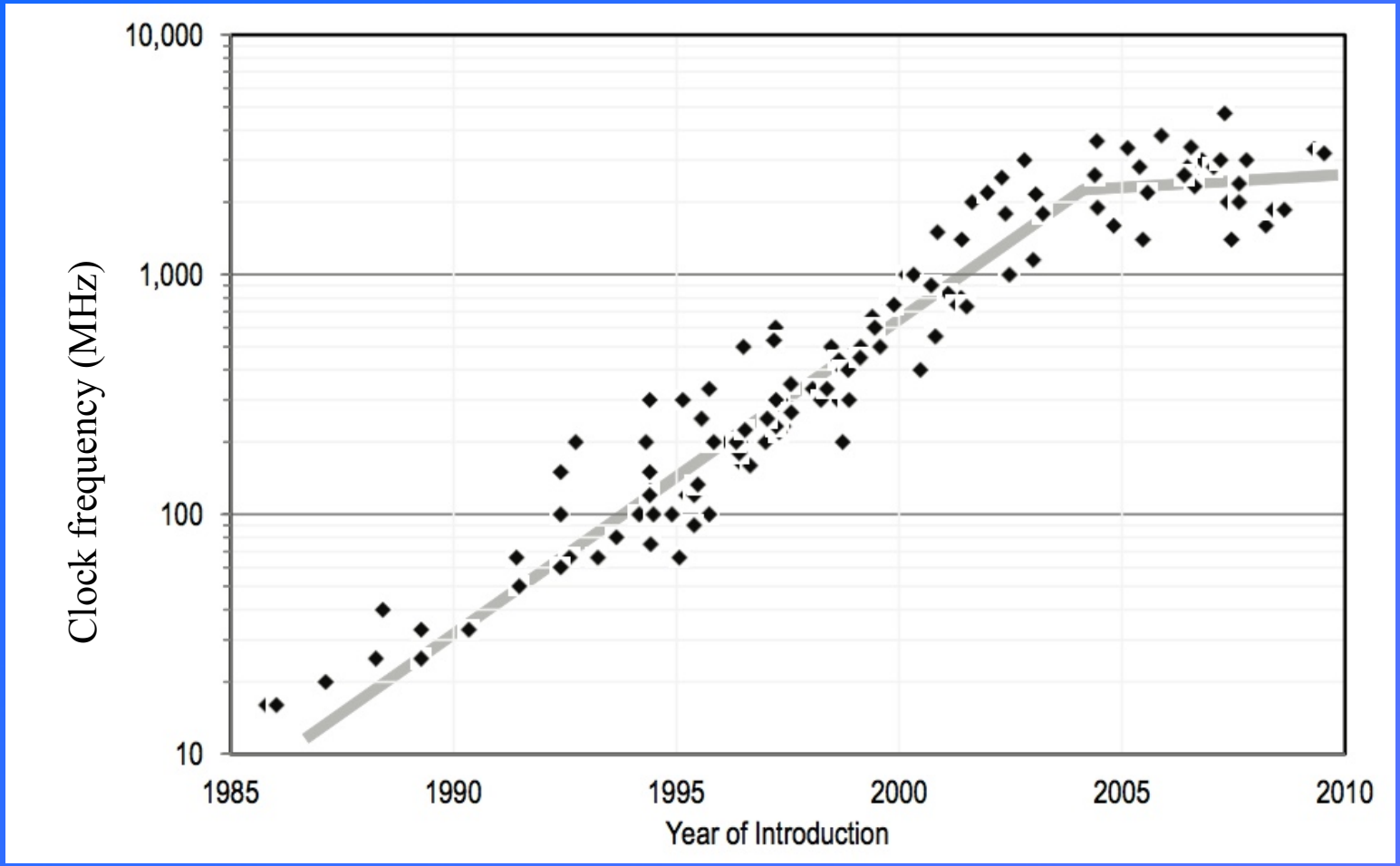


2016 : Apple A10 (TSMC)

3.3 billions of transistors (FinFET)
125mm² (11mm x 11 mm)
4 cores (2 active at a time only)
Technology : 16 nm
Consumption : not released
Clock frequency : 2.34 GHz
2.64 billions of transistors/cm²

Moore's law

Clock frequencies of processors increased from about 10 MHz in 1985 to 3 GHz in 2005 : 40% increase of frequency each year for two decades.

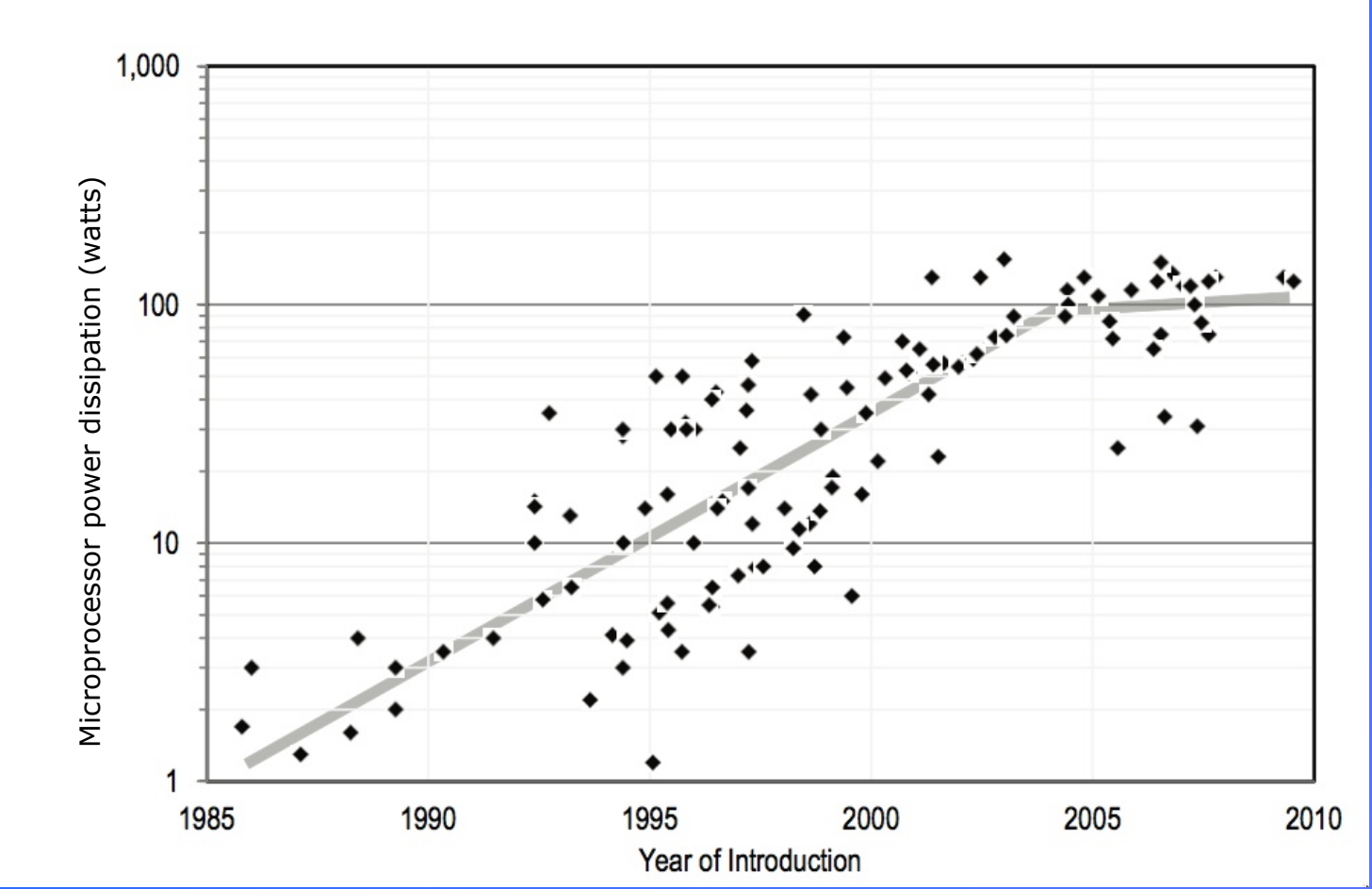


Source : THE FUTURE OF COMPUTING PERFORMANCE - Game Over or Next Level? Copyright 2011 by the National Academy of Sciences of the USA

Dennard scaling law

An equivalent reduction of the power consumption per device is achieved, to keep constant the power dissipated by the chip.

1985 : 1 watt/cm^2 2016 : 145 watts/cm^2



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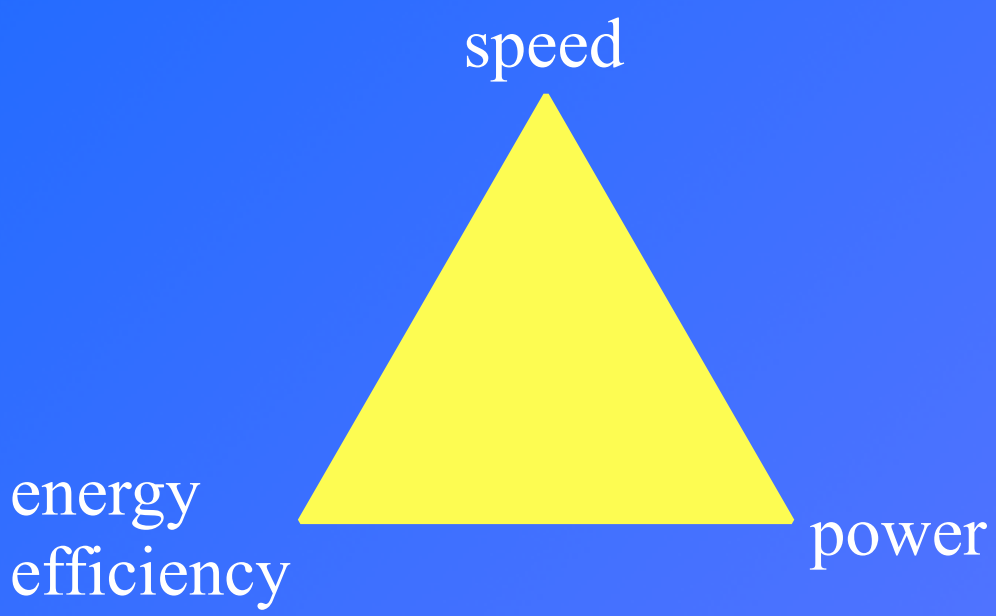
Criteria for technological performance

FLOP : FLoating Point Operation
energy efficiency = number of FLOPs per joule
speed = number of FLOPs per second (speed means frequency of operation)

speed = power * energy efficiency

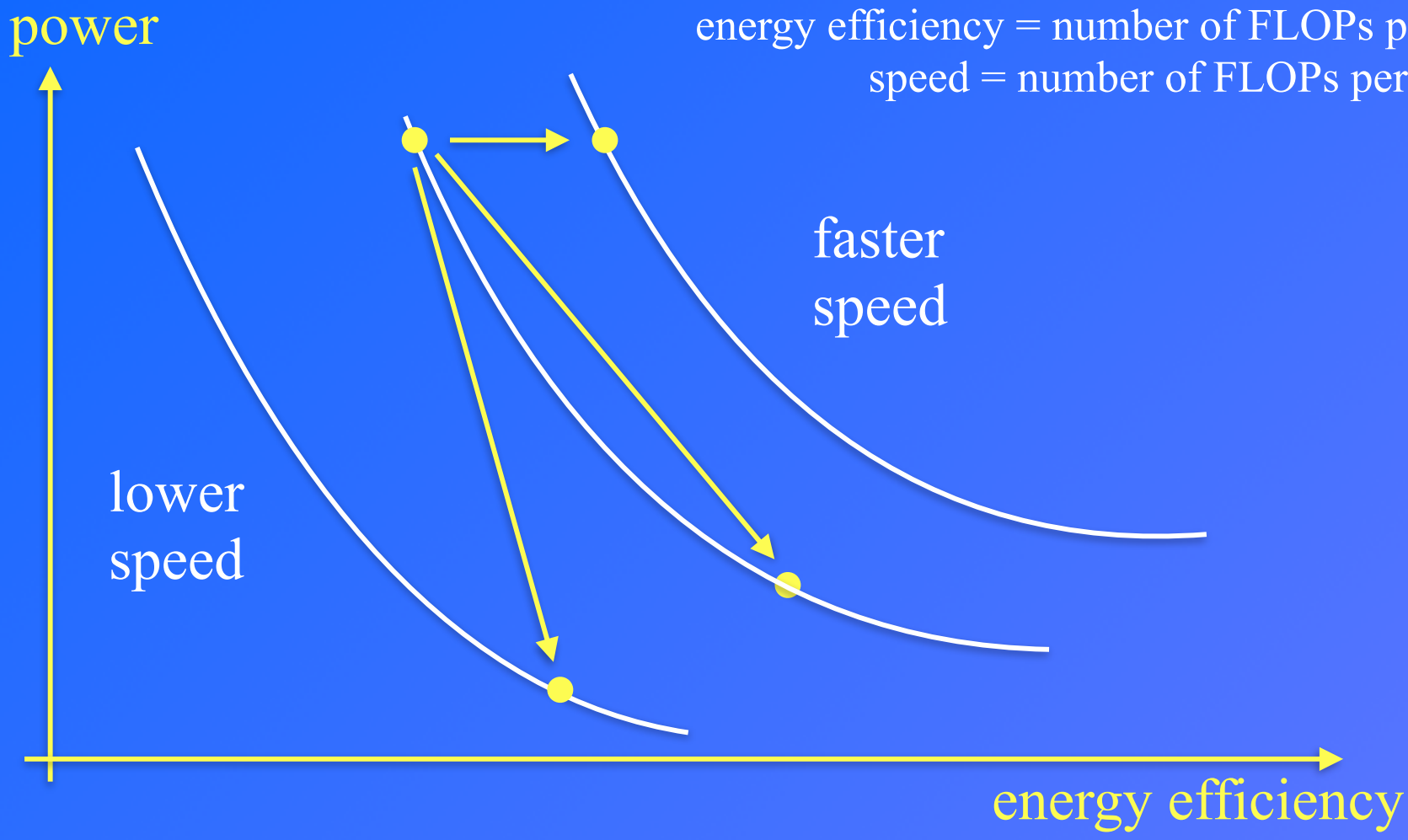


Power versus energy efficiency

speed = power * energy efficiency

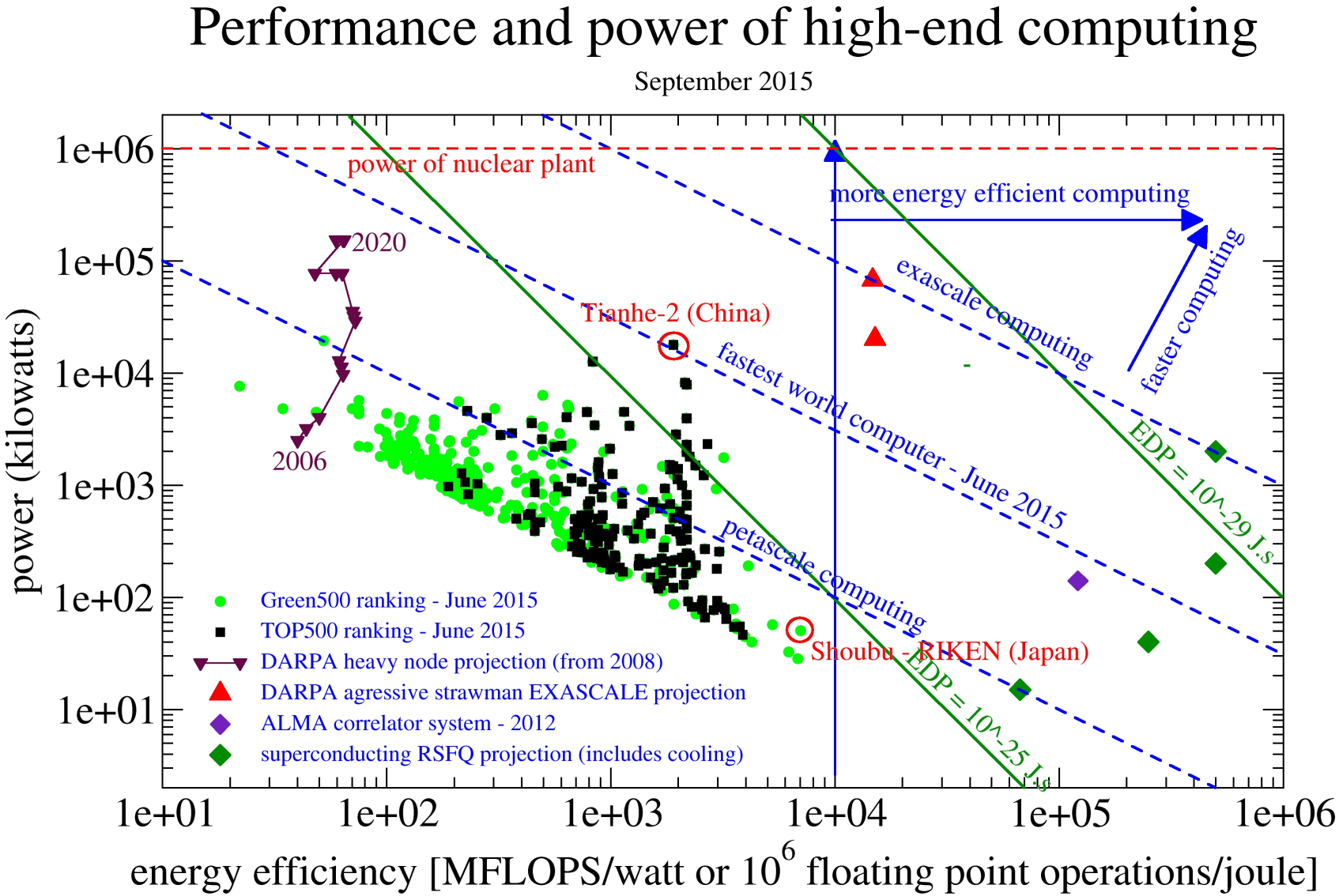
energy efficiency = number of FLOPs per joule

speed = number of FLOPs per second



energy-delay product (EDP) = 1/(energy efficiency * speed) = power/speed^2

Superconductors and semiconductors



Semiconductors : speed and power

Semiconductors : the dynamic power is the limiting quantity :

$$P_{dd} = C\,V_{dd}^2$$

where V_{dd} is the supply voltage and C is the intrinsic gate capacitance.

The intrinsic gate delay is : $\tau = \frac{C\,V_{dd}}{I_d}$

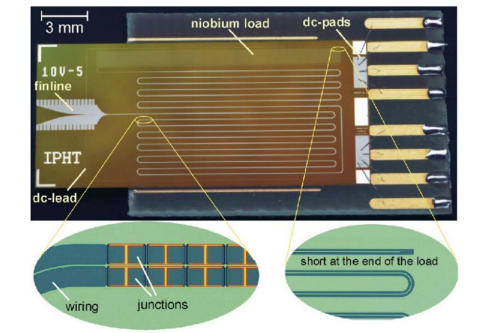
where I_d is the drain saturation current.

The energy-delay product (EDP) is :

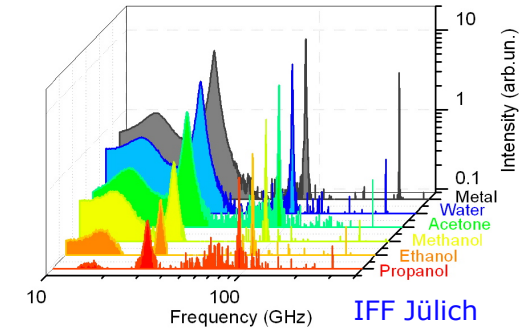
$$EDP = \tau\,P_{dd} = \frac{C\,V_{dd}}{I_d}\,C\,V_{dd}^2 = \frac{C^2\,V_{dd}^3}{I_d}$$

energy-delay product (EDP) = 1/(energy efficiency * speed) = power/speed^2

Superconducting computing with Josephson junctions

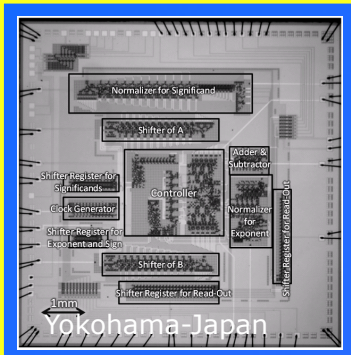


metrology

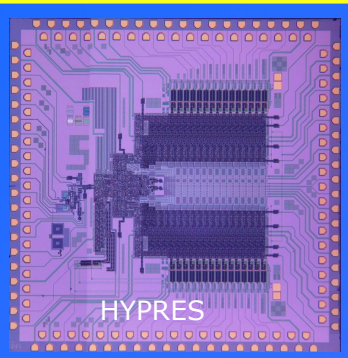


spectroscopy

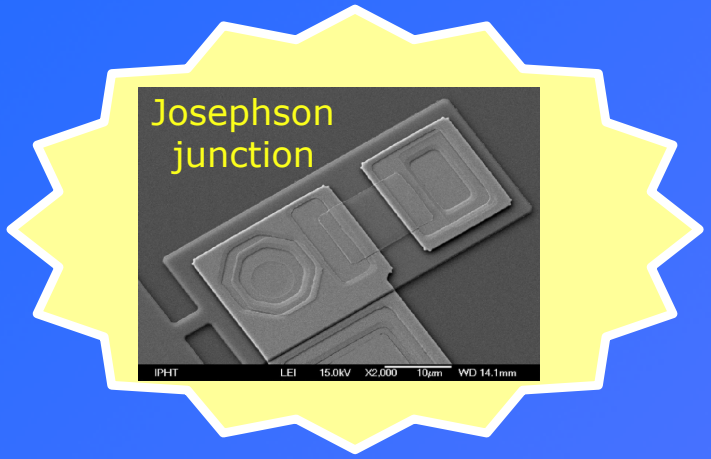
magneto-encephalography

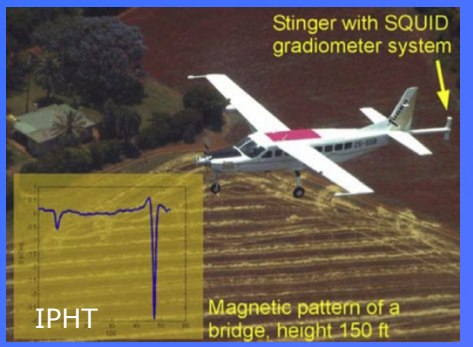


processors

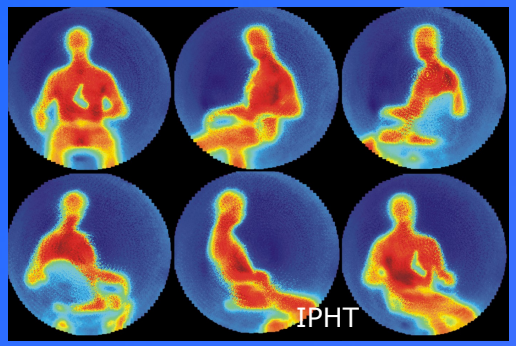


signal processing

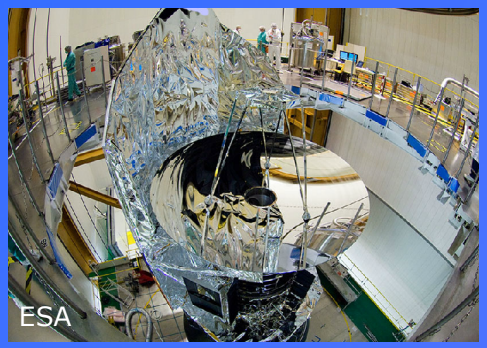




geophysics



security

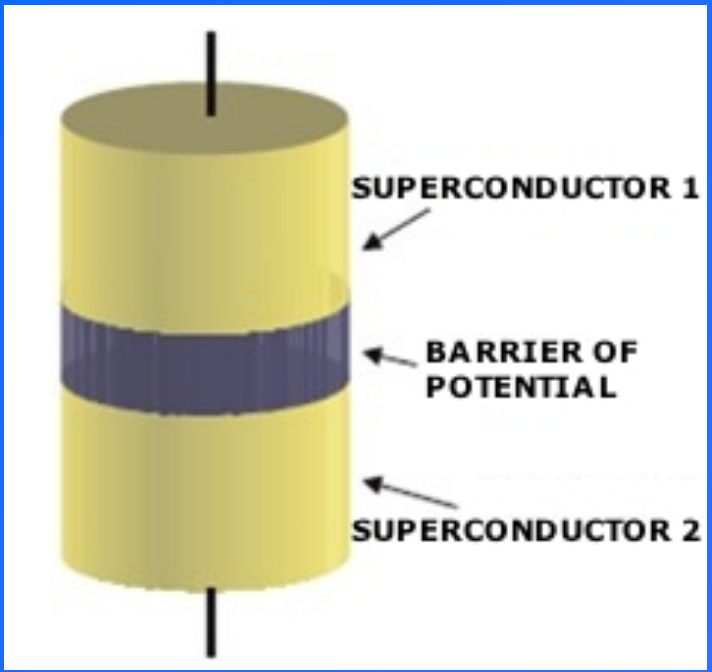


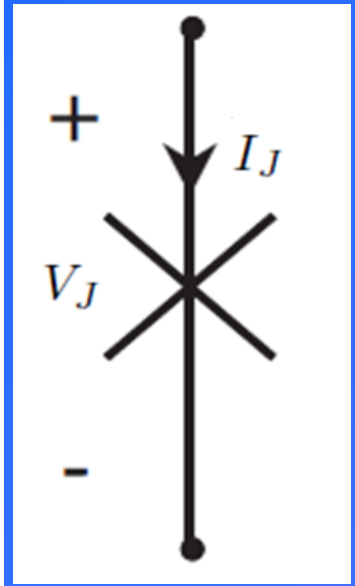
radio-astronomy

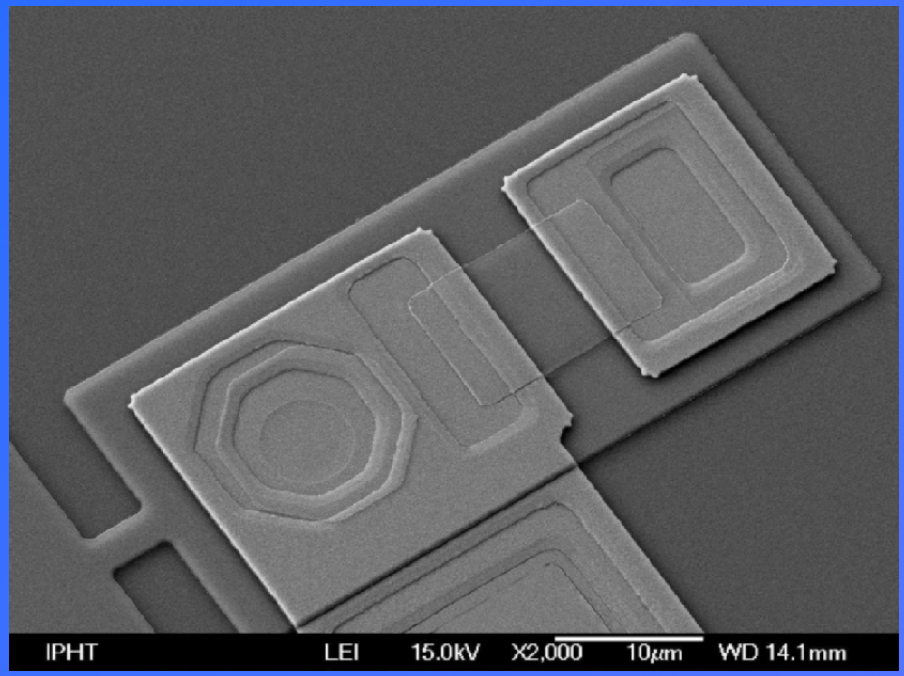
magnetic field imaging

The Josephson junction

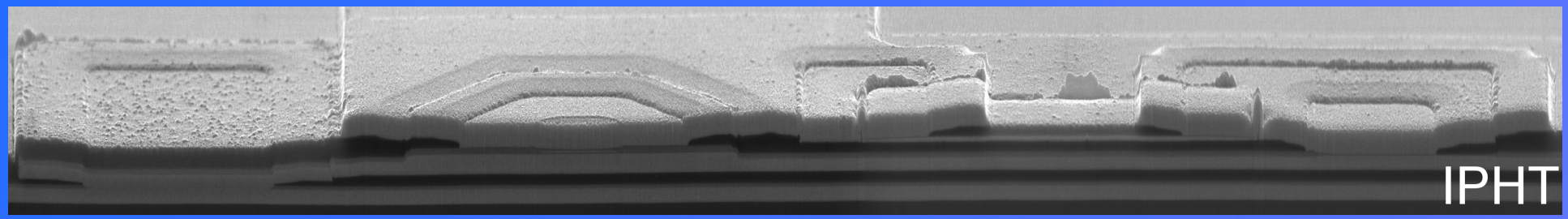
The Josephson junction: the active element of superconductive electronics







Most commonly used materials: Nb/Al-AlOx/Nb @ 4.2 K



3 µm

Pictures from the FLUXONICS Foundry - IPHT Jena - Germany

Superconductors : energy-delay product

$$EDP = \tau_0 P_d = \frac{\Phi_0}{2\pi R_{shunt} I_c} I_c \Phi_0 = \frac{{\Phi_0}^2}{2\pi R_{shunt}}$$

The EDP does not depend on the size of devices for externally-shunted junctions.

The EDP depends on the junction area for self-shunted junctions :

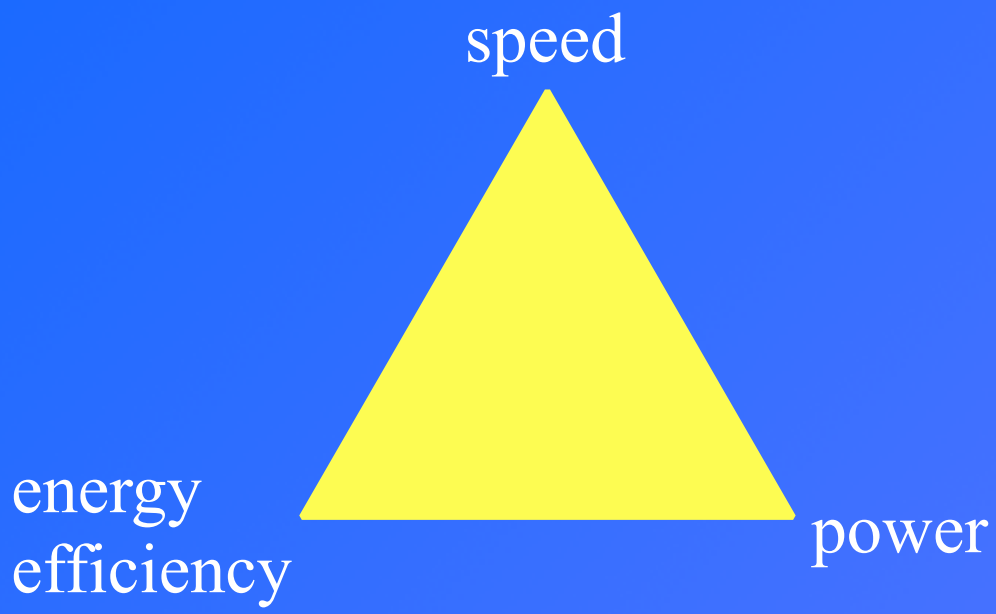
$$EDP \propto \frac{{\Phi_0}^2 A_{JJ}}{2\pi} \approx 10^{-30} \bullet A_{JJ}\left(\mu m^2\right) Joule \cdot Second$$

State of the art :

- chips with 800,000 Josephson junctions (1 cm²)
- clock frequencies up 100 GHz for complex circuits
- 8-bit RISK architecture processors working with clock frequencies of 60 GHz
- consumption of less than 3 mW @4.2K
- 1000 nm-technology

Comparing technologies

speed = power * energy efficiency



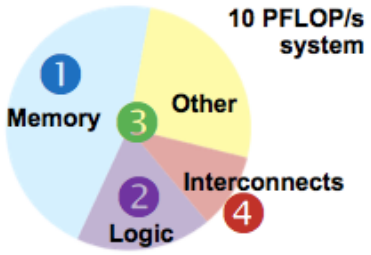
$$EDP(semicon) = \frac{C^2 V_{dd}^3}{I_d}$$

$$EDP(supercon) = \frac{\Phi_0^{\,2}}{2\pi R_{shunt}}$$

energy-delay product (EDP) = 1/(energy efficiency * speed) = power/speed^2

Projet Cryogenic Computer Complexity (C3) - IARPA

Performance (PFLOP/s):	1	10	100	1,000
Power budget (@ 4 K)	1.5 W	10 W	100 W	1,000 W
Logic (RQL, Ic = 25 μA, 8.3 GHz) • processor cores	**0.18** W • 40,200	**1.8** W • 402,000	**18** W • 4,020,000	**180** W • 40,200,000
Memory (1 B/FLOP, JMRAM) • quantity (1 B/FLOPS)	**0.46** W 1 PB	**4.6** W 10 PB	**46** W 100 PB	**460** W 1,000 PB
Interconnects (VCSELs @ 40 K)	**0.1** W	**1** W	**10** W	**100** W
Other (structure, radiation heat leaks)	**0.76** W	**2.6** W	**26** W	**260** W
Total	**1.5** W	**10** W	**100** W	**1,000** W
• Computation efficiency (goal: ≥ 5 x 10^{11} FLOPS/W)	0.7 x 10^{11} FLOPS/W	2.5 x 10^{11} FLOPS/W	**5 x 10^{11}** FLOPS/W	**5 x 10^{11}** FLOPS/W



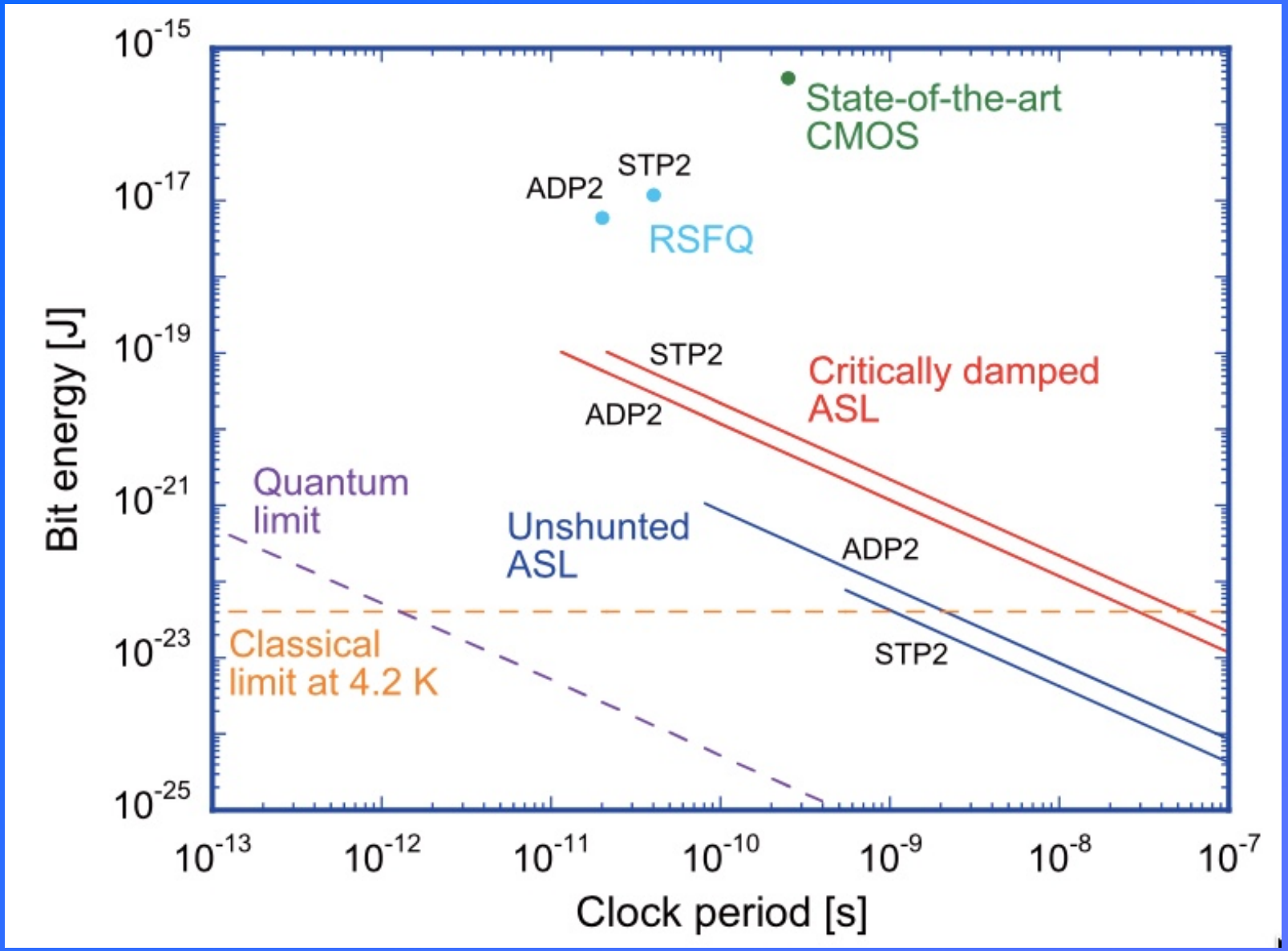
Conclusions:

- Energy-efficient superconducting computers are possible
- Priorities:
  Memory → Logic → System → Interconnects

IEEE Advancing Technology for Humanity

Source: Scott Holmes - présentation Superconducting SFQ VLSI Workshop (SSV 2013) - Novembre 2013

EDP and superconductors



Source : N. Takeuchi et al, "Energy efficiency of adiabatic superconductor logic ", SUST 2015

Superconducting autocorrelators - USA

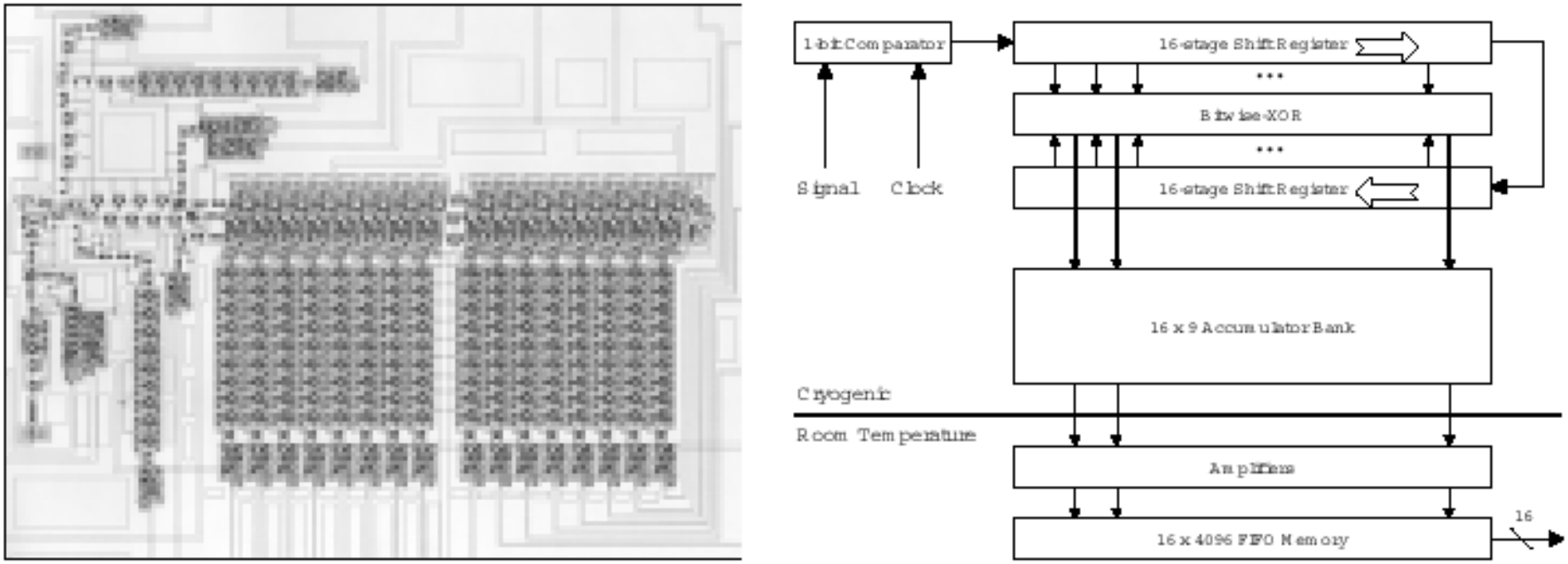


Fig. 42 (left) Mask layout for autocorrelator. (right) Block diagram of autocorrelator.

Source: Darren Brock - Hypres - 2001

16 channels - asynchronous - “dual-rail” logic - 1672 JJ - techno 3500 nm^2
bandwidth: 4 GHz - double oversampling (16 GHz clock)
consumption: < 0.1 mW (i.e. 60 nW/junction)

Superconducting autocorrelators - Japan

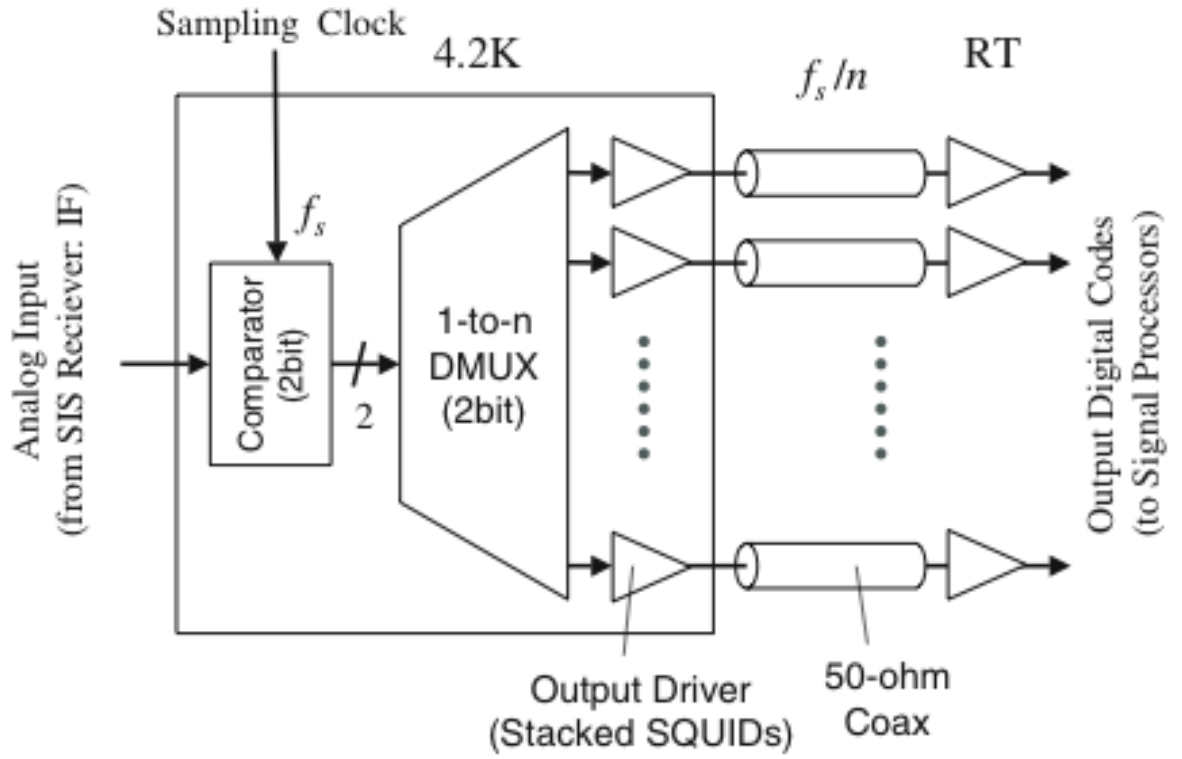


Figure 1. Block diagram of the 2-bit version of the ADC for radio astronomy applications.

Masaaki Maezawa, Motohiro Suzuki, Hitoshi Sasaki and Akira Shoji, "Analog-to-digital converter based on RSFQ technology for radio astronomy applications ," Supercond. Sci. Technol., vol. 14, pp. 1106-1110, 2001